REMARKS

Claims 46-48 and 51-81 are pending in this application. Claims 46-48 have been amended. Claims 49 and 50 have been cancelled without prejudice to their underlying subject matters, which have been incorporated in amended independent claim 46. Claims 72-81 have been added for consideration.

Claims 46-48, 52, 54 and 56-61 stand rejected under 35 U.S.C. §102(b) as being anticipated by Rostoker (U.S. Patent No. 5,662,768) ("Rostoker"). Applicants respectfully traverse this rejection.

The claimed invention relates to semiconductor devices and, in particular, buried conductors within a monocrystalline substrate. As such, amended independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material," and "a conductive path extending from said buried conductor pattern." Amended independent claim 46 also recites "said at least one buried conductor pattern having a spherical pattern." Independent claim 56 recites a buried conductor pattern within a substrate, comprising "at least one empty-spaced pattern in said substrate formed by annealing said substrate containing at least one hole drilled therein" and "a conductive material filling said empty space pattern."

Rostoker relates to "methods of forming high surface area trenches by etching through a substrate having chemically distinct strata." (Col 1, lines 8-10). Rostoker teaches that impurity species are implanted into the substrate "so as to create one or more layers 10 that alternate with unimplanted substrate material 4." (Col 5; lines 15-21; Fig. 1b). Rostoker also teaches that a "preferential etch preferentially removes the impurity-implanted areas with respect to the unimplanted substrate, to form a lateral indentation 16 in the trench sidewalls where the top layer of impurity was implanted." (Col. 6, lines 8-11; Fig. 1e; Fig. 1f). Rostoker notes that "some nonlinearity (high surface area) is introduced in the trench sidewalls." (Col. 6, lines 38-40). Rostoker further teaches that the

"capacitor region includes a layer of oxide 31 or other dielectric conformally deposited on an undulating trench sidewall" (col. 8, lines 61-66) and that the "region of substrate 4 lying immediately beyond the dielectric layer 31 forms one plate of the trench capacitor" while a "plug of polysilicon 32 fills the trench and forms a second plate of the trench capacitor." (Col. 8, line 67; Col. 9, lines 1-3; Fig. 3).

Rostoker does not disclose all limitations of claims 46-48, 52, 54 and 56-61. Rostoker does not teach or suggest an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, said at least one buried conductor pattern *having a spherical pattern*," as amended independent claim 46 recites (emphasis added). Rostoker also does not teach or suggest "at least one empty-spaced pattern in said substrate *formed by annealing said substrate*," as independent claim 56 recites (emphasis added).

As noted above, Rostoker discloses a capacitor with an "undulating trench sidewall," (col. 8, lines 61-66) and not a "buried conductor pattern having a spherical pattern," as amended independent claim 46 recites. Furthermore, Rostoker discloses trenches formed by preferential etching (col. 6, lines 7-11; Fig. 1e) and not "formed by annealing said substrate," as independent claim 56 recites. Accordingly, Rostoker fails to teach or suggest all the limitations of 46-48, 52, 54 and 56-61, and rejection of these claims is respectfully requested.

Claims 46-48, 52, and 54-61 are rejected under 35 U.S.C. §102(b) as being anticipated by Lu et al. (U.S. Patent No. 5,943,581) ("Lu"). Applicants respectfully traverse this rejection.

Lu relates to an integrated circuit semiconductor device and "buried N+ doped region in a silicon substrate which is removed by selective etching to form a cavity," which "is then coated with a dielectric layer and filled with a polysilicon to form a horizontally extending buried reservoir storage capacitor." (Col. 1, lines 19-23).

Lu does not disclose all limitations of claims 46-48, 52, and 54-61. Lu does not teach or suggest an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, said at least one buried conductor pattern *having a spherical pattern*," as amended independent claim 46 recites (emphasis added). Lu also does not teach or suggest "at least one empty-spaced pattern in said substrate *formed by annealing said substrate*," as independent claim 56 recites (emphasis added).

As noted above, Lu discloses a "horizontally extending buried reservoir storage capacitor" (col. 1, lines 22-23) and not a "buried conductor pattern having a spherical pattern," as amended independent claim 46 recites. Furthermore, Lu discloses "selective removal of the N+ doped region 14 by *dry etching* to form a cavity 6 under the device area for the buried reservoir capacitor," (col. 7, lines 17-19; Fig. 6) (emphasis added) and not "at least one empty-spaced pattern in said substrate formed by *annealing* said substrate," as independent claim 56 recites (emphasis added). Accordingly, Lu fails to teach or suggest all the limitations of 46-48, 52, and 54-61, and rejection of these claims is respectfully requested.

Claims 46-48, 51, 52, 56-59 and 61 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,176,789) ("Yamazaki") in view of Yamagata et al. (U.S. Patent No. 5,679,475) ("Yamagata"). Applicants respectfully traverse this rejection.

The subject matter of claims 46-48, 51, 52, 56-59 and 61 would not have been obvious over Yamazaki or Yamazaki in view of Yamagata. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three requirements must be met: (1) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine reference teachings; (2) a reasonable expectation of success; and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. More importantly, the teaching or suggestion to make the claimed

combination and the reasonable expectation for success must both be found in the prior art and not based on Applicant's disclosure. M.P.E.P. § 2142. See, e.g., In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974).

Yamazaki and Yamagata, whether considered alone or in combination, do not teach or suggest all the limitations of amended independent claim 46 or independent claim 56. Yamazaki discloses "a semiconductor device in which a cave is formed in a trench to increase the capacitance formed in the trench." (Col. 4, lines 56-57; Figs. 5(A)-(C)). Yamazaki teaches that "an anisotropic etching [is] carried out to perform a lateral etching so that a cave 40 is formed." (Col. 5, lines 1-2). Yamazaki further teaches that "the cave is desirably formed, in order to increase the inner surface area, like the low portion of a wine-glass," or "the lower profile of the cave may be elongated only in one horizontal direction." (Col. 5, lines 53-58; Figs. 7(A)-(D)). Yamazaki is silent on a "buried conductor pattern *having a spherical pattern*," as amended independent claim 46 recites (emphasis added). Furthermore, Yamazaki teaches that the cave is formed by anisotropic etching and not "formed by *annealing* said substrate," as independent claim 56 recites (emphasis added). Yamagata discloses a semiconductor substrate "characterized by a step of porousifying a silicon monocrystalline substrate to form a porous layer, a step of making a silicon monocrystalline thin film to epitaxially grown on a surface of the porous layer, . . . and a step of selectively etching the porous layer." (Col. 4, lines 25-34). Yamazaki, even when considered in combination with Yamagata, does not teach or suggest all the limitations of independent claims 46 and 56 and their respective dependent claims 47-48, 51, 52, 57-59 and 61. The subject matter of claims 46-48, 51, 52, 56-59 and 61 would not have been obvious over the references and should be considered allowable. Applicants respectfully request that the 35 U.S.C. §103(a) rejection of claims 46-48, 51, 52, 56-59 and 61 be withdrawn.

Claims 46, 47, and 51-54 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Witek et al. (U.S. Patent No. 5,291,438) ("Witek") in view of Yamagata. Applicants respectfully traverse this rejection.

The subject matter of claims 46, 47, and 51-54 would not have been obvious over Witek, or Witek in view of Yamagata. Witek and Yamagata, whether considered alone or in combination, do not teach or suggest all the limitations of amended independent claim 46. Witek relates to "transistor and capacitor structures used in semiconductors, such as memories." (Col. 1, lines 11-13). Witek teaches that a "trench is etched into the substrate 12." (Col. 4, lines 19-20; Fig. 1). Witek also teaches that a "conductive region 14 is formed within the trench." (Col. 4, lines 28-29; Fig. 2). Witek further teaches that "a first capacitor electrode 16 is formed adjacent the trench sidewall and adjacent the sidewall of conductive region 14," and a "capacitor dielectric layer 18 is formed overlying the electrode 16." (Col. 4, lines 47-61; Fig. 3). According to Witek, "a conductive layer 20 is formed overlying the dielectric layer 18." (Col. 4, lines 64-65; Fig. 4). Witek discloses a trench capacitor and not a "buried conductor pattern having a spherical pattern," as amended claim 46 teaches. Witek, even when considered in combination with Yamagata, does not teach or suggest all the limitations of independent claim 46 and dependent claims 47 and 51-54. The subject matter of claims 46, 47 and 51-54 would not have been obvious over the references and should be considered allowable. Applicants respectfully request that the 35 U.S.C. §103(a) rejection of claims 46, 47 and 51-54 be withdrawn.

Claims 62-71 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker and further in view of Tsu et al. (U.S. Patent No. 6,294,420 B1) ("Tsu"). Applicants respectfully traverse this rejection.

Rostoker and Tsu, whether considered alone or in combination, do not teach or suggest all the limitations of independent claim 62. For at least the same reasoning set forth above regarding the patentability of claim 56 as not anticipated by Rostoker, Rostoker would not have rendered the subject matter of independent claim 62 obvious. Independent claim 62 recites "a processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a substrate having at least one empty space pattern formed

by annealing said substrate having at least one hole drilled therein" and "a conductive material filling said empty space pattern." Rostoker does not teach or suggest "having at least one empty space pattern *formed by annealing* said substrate," as claim 62 recites (emphasis added). Tsu discloses an integrated circuit capacitor with a polysilicon plug that is also "formed through conventional patterning and etching." (Col. 5, lines 56-65; Fig. 3a). Hence, the disclosure of Tsu cannot supplement the inadequacies of Rostoker in this regard.

Since Rostoker, even when considered in combination with Tsu, does not teach or suggest all the limitations of independent claim 62 and its dependent claims 63-71, the subject matter of claims 62-71 would not have been obvious over the references. Therefore, claims 62-71 should be considered allowable. Applicants respectfully request that the 35 U.S.C. §103(a) rejection of claims 62-71 be withdrawn.

A marked-up version of the changes made to claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is

respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

46. (Amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, said at least one buried conductor pattern having a spherical pattern, and a conductive path extending from said buried conductor pattern.

47. (Amended) The integrated circuit of claim 46, [wherein said] further comprising a second buried conductor pattern [has] having a pipe-shaped pattern.

48. (Amended) The integrated circuit of claim 46, [wherein said] further comprising a second buried conductor pattern [has] having a plate-shaped pattern.

72. (New) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, said at least one buried conductor pattern having a plate-shaped pattern, and a conductive path extending from said buried conductor pattern.

73. (New) The integrated circuit of claim 73, further comprising a second buried conductor pattern having a pipe-shaped pattern.

74. (New) The integrated circuit of claim 73, further comprising a third buried conductor pattern having a spherical pattern.

75. (New) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, said at least one buried conductor pattern having a pipe-shaped pattern, and a conductive path extending from said buried conductor pattern.

76. (New) An integrated circuit substrate comprising at least two buried conductor patterns provided within a monocrystalline substrate and surrounded by semiconductor material, wherein a first of said at least two buried conductor patterns is

located below a second of said at least two buried conductor patterns and relative to a surface of said monocrystalline substrate, and a first conductive path extending from said first of said at least two buried conductor patterns and a second conductive path extending from said second of said at least two buried conductor patterns.

77. (New) The integrated circuit of claim 76, further comprising a third buried conductor pattern located below said at least two buried conductor patterns and relative to a surface of said monocrystalline substrate and a third conductive path extending from said third buried conductor pattern.

78. (New) The integrated circuit of claim 77, wherein said at least one of buried conductor patterns has a pipe-shaped pattern.

79. (New) The integrated circuit of claim 77, wherein said at least one of buried conductor patterns has a plate-shaped pattern.

80. (New) The integrated circuit of claim 77, wherein said at least one of buried conductor patterns has a spherical pattern.

81. (New) The integrated circuit of claim 77, wherein said conductive patterns are formed of a conductive material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.